WHAT IS CLAIMED IS:

1. A memory module comprising:

a module substrate;

at least one command-address signal register;

a plurality of memory chips provided on a top face and under face of the module substrate, each of the plurality of memory chips having a command-address signal terminal with an active-termination circuit; and

command-address signal wiring,

wherein the command-address signal register is internally wired and connected to the plurality of memory chips,

wherein the plurality of memory chips is divided so as to form at least one 1-ranked memory group including two or three memory chips that are provided on one face and the other face of the module substrate and near and adjacent to each other and at least one 2-ranked memory group including two or three memory chips that are provided on one face and the other face of the module substrate and near and adjacent to each other,

wherein the 1-ranked memory group is paired with the 2-ranked memory group adjacent thereto so that this pair of memory groups has four or five memory chips,

wherein the command-address signal wiring has a T-branch structure and is used for connecting the command-address signal register to the pair of memory groups corresponding thereto, and

wherein when access is made, one of the pair of memory groups is used during the access and the other is not used and the command-address signal terminals of the memory chips of the memory group that is not used during the access are actively terminated.

2. A memory module according to Claim 1, further comprising data signal wiring with T-branch structure for connecting one of the pair of

memory groups to the other,

wherein each of the plurality of memory chips further has a data-signal terminal, and

wherein the data-signal terminals of the memory chips of the memory group that is not used during the access are actively terminated.

3. A memory module according to Claim 1, further comprising command-address active-termination control signal wiring connected to a module terminal corresponding to any of the memory groups.

4. A memory module according to Claim 1, further comprising clock-signal wiring with a T-branch structure,

wherein each of the plurality of memory chips further has a clock signal terminal,

wherein an even-number of the command-address signal registers are provided so as to form at least two groups, wherein the clock-signal wiring is connected to the command-address signal registers and the memory chips so as to connect the at least two groups of command-address signal registers to each other and the pair of memory groups to each other, and

wherein the clock-signal terminals of the memory chips of one of the pair of memory groups are actively terminated.

5. A memory module according to Claim 1, wherein each memory group of at least one of the pairs of memory groups adjacent and connected to each other so as to form a T-branch structure has two stacked memory chips on one face of the module substrate and one memory chip on the other face of the module substrate and wherein the command-address signal terminal of the memory chip on the other face is actively terminated.

6. A memory module according to Claim 5, wherein four pairs of the memory groups with error checking and correcting (ECC) capability including six memory groups, each of the six memory groups having one memory chip on one face of the module substrate and another memory chip on the other

face of the module substrate, and two memory groups, each of the two memory groups having two memory chips stacked on each other on one face of the module substrate and another memory chip on the other face of the module substrate.

7. A memory module according to Claim 5, wherein the stacked memory chips include a single memory chip with a first pad provided on one face of a printed circuit board and another single memory chip with a second pad provided on the other face of the printed circuit board, wherein the command-address signal wiring is connected to both the first and second pads through a single wire and the data-signal wiring is connected to one of the first and second pads through another single wire, and wherein a signal line of the stacked memory chips is sandwiched between a power layer and a ground layer so as to form a strip line.

8. A memory module according to Claim 1, further comprising a wiring-impedance matching resistor, wherein the at least one command-address signal register is provided under the plurality of memory chips and the wiring-impedance matching resistor is inserted in wiring with a T-branch structure connected to the command-address signal terminals.

9. A memory module according to Claim 1, further comprising clock-signal wiring with a T-branch structure for connecting one of the memory groups paired with each other to the other, wherein memory chips of one of the pair of memory groups are terminated.

10. A memory module according to Claim 1, wherein each of the plurality of memory chips further has an active-termination circuit for a command-address active-termination control signal, a circuit for latching the command-address active-termination control signal, and a circuit for turning at least part of the active-termination circuit when the command-address active-termination control signal is latched during the active-termination circuit is turned on.

11. A memory chip used for a memory module having at least one command-address signal register and a plurality of memory chips mounted on the memory module, each of the plurality of memory chips having a command-address signal terminal with an active-termination circuit, wherein the command-address signal register is internally wired and connected to the plurality of memory chips, the memory chip comprising:

an active-termination circuit for a command-address active-termination control signal;

a circuit for latching the command-address active-termination control signal; and

a circuit for turning off at least part of the active-termination circuit when the command-address active-termination control signal is latched during the active-termination circuit is turned on.

12. A memory system comprising:

a mother board;

first and second memory modules according to Claim 1 provided on the mother board; and

a memory controller connected to a plurality of memory chips mounted on the two memory modules so as to control memory capability,

wherein a signal wirings between each of the memory modules and the memory controller are independently connected therebetween.

13. A memory system according to Claim 12, wherein the first memory module is provided at a first distance from the memory controller and the second memory module is provided at a second distance longer than the first distance from the memory controller, and wherein signal wiring from the first memory module to the memory controller is formed as internal-layer wiring and signal wiring from the second memory module to the memory controller is formed as surface-layer wiring.

14. A memory system comprising:

a mother board;

first and second memory modules according to Claim 1 provided on the mother board; and

a memory controller connected to a plurality of memory chips mounted on the two memory modules so as to control memory capability,

wherein, among signal wirings connecting between each of the memory modules and the memory controller, at least one of the command-address signal and the clock signal is connected through wiring with a T-branch structure near the memory modules on the mother board.